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DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Abstract of the Disclosure

Structures and methods for improving sense amplifier operation are provided. A first embodiment includes a sense amplifier having a pair of cross-coupled inverters. Each inverter includes a transistor of a first conductivity type and a pair of transistors of a second conductivity type which are coupled at a drain region and are coupled at a source region. The drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type. A pair of input transmission lines are included where each one of the pair of input transmission lines is coupled to a gate of a first one of the pair of transistors in each inverter. A pair of output transmission lines is included where each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

High performance, wide bandwidth or very fast CMOS amplifiers are possible using the new circuit topology of the present invention. The new modified sense amplifier for low voltage DRAMs is as much as 100 times faster than a conventional voltage sense amplifier when low power supply voltages, e.g. Vdd less than 1.0 Volts, are utilized. In the novel sense amplifier, the bit line capacitance is separated from the output nodes of the sense amplifier.